ABSTRACT

The output (θ2) of a digital adder (13) before being held by a first data holding circuit (14), a first reference value (D1) and a second reference value (D2) are compared, respectively, by a first data comparator (15) and a second data comparator (16), to thereby change one cycle of the output control of the pulse train fout from four cycles (T1-T4) to two cycles (T1-T2) of the reference clock. Further, by comparing the output (θ1) of the first data holding circuit (14) and the first reference value (D1) by a third data comparator (19), the latch timing of the overflow signal is changed from T4 to T1.